REMARKS

Applicant respectfully requests reconsideration and allowance in view of the following remarks. In the Office Action, mailed June 10, 2004, the Examiner rejected claims 1-9 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,412,028 to Steed et al. For the reasons stated below, Applicant respectfully disagrees with the Examiner's rejections and Applicant requests allowance of claims 1-9.

Regarding independent claim 1, the Examiner equates the second processor of the present application with an implied processor, supposedly located in an external device and connected to a host computer system by a cable (Steed at col. 5, lines 4-6 and lines 17-22). While acknowledging that Steed discloses no second processor, the Examiner suggests that the USB device must be a processor "to execute DMA operations without the use of the host processor." Applicant agrees with the Examiner that there is no explicit support for this latter construction and observes that Steed explicitly locates the virtual DMA software in the host system ("the USB interface code 226 includes the virtual DMA software" at col. 7, lines 41-42). Applicant also notes the distinct absence of a processor in Figure 3 of Steed, a drawing that depicts the USB-DAQ device.

Further, Steed teaches away from a second processor when it states that the USB device may be "***speakers***" or one of several listed primitive devices, many of which, it will be appreciated, do not require an on-board processor susceptible to programming or capable of executing virtual DMA code (col. 5, lines 17-22). Thus, Steed most clearly and reasonably describes a computer system that executes virtual DMA software within the computer system and connects to an external USB device (Figures 3 and 4; col. 6, line 63 - col. 7, line 60).

Even if the USB device possessed a qualifying second processor, it is difficult to reconcile the stated goals of Steed with the functionalities enabled by aspects of the present application. For example, claim 1 provides that:

> the software DMA engine, when executed by a processor of the first and second processors, being capable of transferring data directly between all resources in the computer system.

It will be apparent to one skilled in the art, and readily appreciated after reviewing Figure 2 of Steed, that a second processor located on the USB device would not have direct access to all resources on the host system. Nor would the processor in Steed have direct access to all resources in the USB device. The USB connection requires intermediate software and hardware

that prevents direct connection between the Steed processor and the USB device controlling circuitry (Steed, Figure 2 and col. 6, lines 24-34). Therefore, neither the first processor nor an alleged second processor of Steed would be capable of transferring data directly between all resources as required by claim 1 of the present application.

Finally, it is an express goal of the Steed invention to increase USB data transfer rates with minimal changes to DAQ driver level software (col. 3, lines 56-58). In contrast, aspects of the present invention address limitations and problems with typical DMA controllers that are used to improve performance of DRAM memory. It will be appreciated that the access speeds of DRAM memory are typically orders of magnitude faster than access speeds of devices connected by USB. It is clear, therefore, that the combination of a slow USB connection and a purported second processor accessible through the USB connection cannot reasonably be considered anticipatory of the present invention.

Therefore, it is apparent that Steed does not describe each and every element as set forth in claim 1. Steed addresses problems related to the transfer of data from a peripheral over a relatively slow serial bus. Steed cannot reasonably be considered to require "a processor of the first and second processors" that executes a software DMA engine being capable of transferring data directly between all resources in the computer system. Thus, the Steed reference does not anticipate the present invention and the rejection to claim 1 should be withdrawn.

Regarding independent claim 6, the Examiner provided no basis for rejection of each and every element of the claim and the rejection should therefore be withdrawn. However, Applicant respectfully requests withdrawal of the rejection of claim 6 for the reasons stated above (regarding the rejection of claim 1) and the arguments stated below that address the Examiner's rejection of claims 5 and 6.

Regarding claims 5 and 6, the Examiner rejects claims 5 and 6 alleging that "Steed teaches the loading of multiple data packets from a device and storing these multiple packets into the system memory." However, claims 5 and 6 provide a load multiple data instruction that writes data to multiple locations in internal registers (claim 6 recites "an internal register") and a store multiple data instruction that transfers data from multiple locations in the internal registers (claim 6 recites "in the internal register"). Steed does not provide for reading data from, or writing data to, internal registers of a processor. The DMA emulator of Steed operates by "...'fooling' the DAQ driver level software into thinking the data is being acquired from the device using DMA" (col. 4, lines 19-22). This "fooling" enables Steed to preserve existing DAQ

drivers with little or no changes (col. 4 at lines 22-25). As can be appreciated by one skilled in the art, a hardware DMA device would preclude the movement of data directly to the internal registers of the Steed processor, since DMA provides for data transfer independent of a processor (see Wikipedia at http://en.wikipedia.org/wiki/Direct_memory_access). Consequently, a DMA emulator that minimizes device driver changes would not move data to or from internal registers. Therefore, Steed cannot be said to anticipate the operation of the load multiple data instruction and the store multiple data instruction as recited in claims 5 and 6, and the rejection of claims 5 and 6 should be withdrawn.

Regarding claims 2 and 9, Steed provides a DMA emulator that functions cooperatively with a DAQ driver and a serial bus (USB) driver (col. 3, lines 51-55). Additionally, a USB device is provided for handling the USB interface (see col. 6, lines 24-35) and Steed provides for the preservation of existing DAQ drivers with little or no changes (col. 4, at lines 22-25). Therefore, it is clear from the specification of Steed that USB data and control, including reformatting, is handled by USB hardware and drivers. Further, it is apparent that a DMA emulator engaged in data processing, data filtering, data compacting and data reformatting would be contrary to the stated objectives of Steed because such a DMA emulator would necessitate the modification of driver software to accommodate the data mutation. For at least these reasons, Applicant respectfully disagrees with the Examiner that the processing of data is inherently taught by Steed and accordingly requests withdrawal of the rejections of claims 2 and 9.

Regarding claims 3 and 7, Applicant replies that since claim 3 depends from allowable claims 1-2 and claim 7 depends from allowable claim 6, claims 3 and 7 are also allowable and refers Examiner to the previous arguments relevant to claims 1-2 and 6.

Regarding claims 4 and 8, Applicant respectfully disagrees with the assertion that Steed teaches the presently claimed "one or more hardware buffers, in combination with the software DMA engine, permit the one or more peripherals to access the memory directly." The cited passage in Steed speaks of a "user buffer," defining the buffer as being "the buffer in computer memory used by the driver software and/or application" (col. 9, lines 39-48). This latter definition explicitly provides access to memory by driver software and application software; Steed makes no provision for hardware buffers that permit one or more peripherals to access memory directly. Therefore, Steed does not anticipate the subject matter of claims 4 and 8 and Applicant respectfully requests withdrawal of the rejections of claims 4 and 8.

In summary, for at least the reasons presented above, Steed does not teach or suggest software Direct Memory Access software in a system comprising two or more processors as claimed in the present application. Accordingly, Applicant respectfully submits that claims 1-9 are allowable over the art of record.

CONCLUSION

Applicant has addressed the claim rejections under 35 U.S.C. §102. Applicant believes all claims are in condition for allowance.

If any further questions should arise prior to a Notice of Allowance, the Examiner is invited to contact the attorney at the number set forth below.

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Respectfully submitted,

David H. Jaffer
Reg. No. 32,243
Customer No. 27498

PILLSBURY WINTHROP LLP
2475 Hanover Street
Palo Alto, CA 94304-1114
Tel. No. 650-233-4510
djaffer@pillsburywinthrop.com

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on 12-7, 2004 by Diana Dearing.

Diana Dearing